In The Claims:

The listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (currently amended) A method of bumping a substrate including a metal layer thereon wherein the metal layer has an exposed portion, the method comprising:

forming a barrier layer comprising a barrier layer material on the substrate ~~including~~ and on the exposed portion of the metal layer;

forming a conductive bump comprising a conductive bump material on the barrier layer wherein the barrier layer is between the conductive bump and the substrate and wherein the conductive bump is laterally offset and laterally separated from the exposed portion of the metal layer in a direction parallel to a surface of the substrate so that the exposed portion of metal layer is free of the conductive bump material; and

after forming the conductive bump, removing ~~at least some of~~ the barrier layer from the exposed portion of the metal layer ~~thereby exposing the metal layer~~ while maintaining a portion of the barrier layer between the conductive bump and the substrate so that the portion of the barrier layer maintained between the conductive bump and the substrate is laterally offset and laterally separated from the exposed portion of the metal layer in the direction parallel to the surface of the substrate and so that the exposed portion of the metal layer is free of the barrier layer material.

2. (original) A method according to Claim 1 wherein the substrate comprises an integrated circuit substrate.

3. (original) A method according to Claim 1 wherein the metal layer comprises an aluminum layer.

4. (original) A method according to Claim 1 wherein the barrier layer comprises a layer of TiW.

5. (original) A method according to Claim 1 wherein the metal layer, the barrier layer, and the conductive bump all comprise different materials.

6. (currently amended) A method according to Claim 1 further comprising:

before forming the conductive bump, forming a conductive under bump metallurgy layer on the barrier layer; and

before removing the barrier layer, removing the conductive under bump metallurgy layer from the barrier layer opposite the metal layer while maintaining a portion of the conductive under bump metallurgy layer between the conductive bump and the substrate so that the portion of the conductive under bump metallurgy layer maintained between the conductive bump and the substrate is laterally offset and laterally separated from the exposed portion of the metal layer in the direction parallel to the surface of the substrate and so that the exposed portion of the metal layer is free of the conductive under bump metallurgy layer.

7. (original) A method according to Claim 6 wherein the conductive under bump metallurgy layer comprises copper.

8. (original) A method according to Claim 6 wherein the conductive under bump metallurgy layer and the barrier layer comprise different materials.

9. (original) A method according to Claim 6 further comprising:

before forming the conductive bump, forming a second barrier layer on the under bump metallurgy layer wherein the second barrier layer and the under bump metallurgy layer comprise different materials and wherein the second barrier layer is between the conductive bump and the conductive under bump metallurgy layer.

10. (original) A method according to Claim 9 wherein the second barrier layer comprises nickel.

11. (original) A method according to Claim 10 wherein the under bump metallurgy layer comprises copper.

12. (currently amended) A method according to Claim 9 wherein forming the second barrier layer comprises selectively forming the second barrier layer on a portion of the under bump metallurgy layer wherein the second barrier layer is laterally offset and laterally separated from the exposed portion of the metal layer in a direction parallel to the surface of the substrate.

13. (currently amended) A method according to Claim 12 wherein forming the conductive bump comprises selectively forming the conductive bump on the second barrier layer laterally offset and laterally separated from the exposed portion of the metal layer in a direction parallel to the surface of the substrate.

14. (original) A method according to Claim 13 wherein selectively forming the second barrier layer and selectively forming the conductive bump comprise selectively forming the second barrier layer and the conductive bump using a same mask.

15. (original) A method according to Claim 1 wherein the conductive bump comprises at least one of solder, gold, and/or copper.

16. (currently amended) A method according to Claim 1 wherein forming the conductive bump comprises selectively plating the bump on the barrier layer laterally offset and laterally separted from the exposed portion of the metal layer in a direction parallel to the surface of the substrate.

17. (original) A method according to Claim 1 wherein the integrated circuit substrate includes an input/output pad thereon, wherein the barrier layer is formed on the substrate including the metal layer and the input/output pad, and wherein the conductive bump is formed on the barrier layer opposite the input/output pad.

18. (original) A method according to Claim 17 wherein the metal layer and the bump pad both comprise aluminum.

19. (currently amended) A method according to Claim 1 wherein the substrate includes an input/output pad thereon, wherein the barrier layer is formed on the substrate including the metal layer and the input/output pad, and wherein after removing the barrier layer from the exposed portion of the metal layer, the conductive bump is electrically coupled to the input/output pad.

20. (original) A method according to Claim 19 wherein the metal layer and the input/output pad both comprise aluminum.

21. (original) A method according to Claim 19 wherein the conductive bump is formed on the barrier layer opposite the input/output pad.

22. (currently amended) A method according to Claim 19 wherein the conductive bump is laterally offset from the input/output pad in a direction parallel to the surface of the substrate.

23. (currently amended) A method according to Claim 1 further comprising:

after removing the barrier layer from the exposed portion of the metal layer, bonding a second substrate to the conductive bump.

Claims 24-35 (canceled).

36. (currently amended) A method of bumping an electronic device comprising a substrate including ~~an exposed metal~~ a metal layer thereon wherein the metal layer has an exposed portion, the method comprising:

forming a barrier layer comprising a barrier layer material on the substrate wherein the barrier layer is laterally offset and laterally separated from the exposed portion of the metal layer in a direction parallel to a surface of the substrate so that the exposed portion of the metal layer is free of the barrier layer material; and

forming a conductive bump comprising a conductive bump material on the barrier layer wherein the barrier layer is between the conductive bump and the substrate, wherein the conductive bump is laterally offset and laterally separated from the exposed portion of the metal layer in a direction parallel to the surface of the substrate so that the exposed portion of the metal layer is free of the conductive bump material, and wherein the barrier layer, the conductive bump, and the metal layer all comprise different conductive materials.

37. (original) A method according to Claim 36 wherein the electronic device comprises an integrated circuit device, and wherein the substrate comprises an integrated circuit substrate.

38. (original) A method according to Claim 36 wherein the barrier layer comprises titanium tungsten.

39. (original) A method according to Claim 38 wherein the exposed metal layer comprises aluminum.

40. (original) A method according to Claim 38 wherein the conductive bump comprises at least one of solder, gold, and/or copper.

41. (original) A method according to Claim 36 further comprising:

forming a conductive under bump metallurgy layer between the barrier layer and the conductive bump.

42. (original) A method according to Claim 36 further comprising:

bonding a second substrate bonded to the conductive bump.

43. (original) A method according to Claim 36 wherein the integrated circuit substrate includes an input/output pad thereon and wherein the barrier layer and the conductive bump are electrically connected to the input/output pad.

44. (original) A method according to Claim 43 wherein the input/output pad and the metal layer each comprise aluminum.

45. (original) A method according to Claim 43 wherein the conductive bump is on the barrier layer opposite the input/output pad.

46. (currently amended) A method according to Claim 43 wherein the conductive bump is laterally offset from the input/output pad in a direction parallel to the surface of the substrate.

47. (original) A method according to Claim 36 further comprising:

an under bump metallurgy layer between the barrier layer and the conductive bump wherein the under bump metallurgy layer and the barrier layer comprise different materials.

48. (currently amended) A method of bumping an integrated circuit substrate including a metal layer thereon wherein the metal layer has an exposed portion, the method comprising:

forming a barrier layer on a substrate ~~including~~ and on the exposed portion of the metal layer;

forming a conductive bump on the barrier layer wherein the barrier layer is between the conductive bump and the substrate and wherein the conductive bump is laterally offset and laterally seprated from the metal layer in a direction parallel to a surface of the substrate; and

after forming the conductive bump, removing the barrier layer from the exposed portion of the metal layer ~~thereby exposing the metal layer~~ while maintaining a portion of the barrier layer between the conductive bump and the substrate so that the portion of the barrier layer maintained between the conductive bump and the substrate is laterally separated from the metal layer in a direction parallel to the surface of the substrate.

Claim 49 (canceled).

50.(new) A method according to Claim 1 wherein removing the barrier layer further comprises removing the barrier layer from portions of the substrate surrounding the exposed portion of the metal layer.

51.(new) A method according to Claim 36 wherein portions of the substrate surrounding the exposed portion of the metal layer are free of the barrier layer material.

52.(new) A method according to Claim 48 wherein removing the barrier layer further comprises removing the barrier layer from portions of the substrate surrounding the exposed portion of the metal layer.

53. (new) A method of bumping an electronic device comprising a substrate including a metal layer wherein the metal layer has an exposed portion, the method comprising:

forming a barrier layer comprising a barrier layer material on the substrate wherein the exposed portion of the metal layer and portions of the substrate surrounding the exposed portion of the metal layer are free of the barrier layer material; and

forming a conductive bump comprising a conductive bump material on the barrier layer wherein the barrier layer is between the conductive bump and the substrate, wherein the exposed

portion of the metal layer and portions of the substrate surrounding the exposed portion of the metal layer are free of the conductive bump material, and wherein the barrier layer, the conductive bump, and the metal layer all comprise different conductive materials.

54. (new) A method according to Claim 53 wherein the electronic device comprises an integrated circuit device, and wherein the substrate comprises an integrated circuit substrate.

55. (new) A method according to Claim 53 wherein the barrier layer comprises titanium tungsten.

56. (new) A method according to Claim 55 wherein the exposed metal layer comprises aluminum.

57. (new) A method according to Claim 55 wherein the conductive bump comprises at least one of solder, gold, and/or copper.

58. (new) A method according to Claim 53 further comprising:

forming a conductive under bump metallurgy layer between the barrier layer and the conductive bump.

59. (new) A method according to Claim 53 further comprising:

bonding a second substrate bonded to the conductive bump.

60. (new) A method according to Claim 53 wherein the integrated circuit substrate includes an input/output pad thereon and wherein the barrier layer and the conductive bump are electrically connected to the input/output pad.

61. (new) A method according to Claim 60 wherein the input/output pad and the metal layer each comprise aluminum.

62. (new) A method according to Claim 60 wherein the conductive bump is on the barrier layer opposite the input/output pad.

63. (new) A method according to Claim 60 wherein the conductive bump is laterally offset from the input/output pad in a direction parallel to the surface of the substrate.

64. (new) A method according to Claim 53 further comprising:

an under bump metallurgy layer between the barrier layer and the conductive bump wherein the under bump metallurgy layer and the barrier layer comprise different materials.